Autonomous Bit Error Rate Testing at Multi-Gbit/s Rates Implemented in a 5AM SiGe Circuit for Radiation Effects Self Test (CREST)

Paul Marshall, *Member, IEEE*, Marty Carts, *Member, IEEE*, Steve Currie, Robert Reed, *Member, IEEE*, Barb Randall, Karl Fritz, Krystal Kennedy, Melanie Berg, Ramkumar Krithivasan, Christina Siedleck, Ray Ladbury, *Member, IEEE*, Cheryl Marshall, John Cressler, *Member, IEEE*, Guofu Niu, *Senior Member, IEEE*, Ken LaBel, *Member, IEEE*, and Barry Gilbert, *Fellow, IEEE*

***Abstract*—SEE testing at multi-Gbit/s data rates has traditionally involved elaborate high speed test equipment setups for at-speed testing. We demonstrate a generally applicable self test circuit approach implemented in IBM's 5AM SiGe process, and describe its ability to capture complex error signatures during circuit operation at data rates exceeding 5 Gbit/s. Comparisons of data acquired with FPGA control of the CREST ASIC versus conventional bit error rate test equipment validate the approach. In addition, we describe SEE characteristics of the IBM 5AM process implemented in five variations of the D flip-flop based serial register. Heavy ion SEE data acquired at angles follow the traditional RPP-based analysis approach in one case, but deviate by orders on magnitude in others, even though all circuits are implemented in the same 5AM SiGe HBT process.**

***Index Terms*—Built in self test, high speed bit error rate testing SiGe, single event effects (SEEs).**

I. Introduction

WE have been investigating Silicon Germanium (SiGe) BiCMOS technology for its high performance characteristics for nearly a decade, and the technology has shown great promise for high speed digital as well as mixed-signal applications. This technology offers a high speed heterojunction bipolar transistor (HBT) that is integrated with more conventional CMOS transistors. Beginning in 2000, we have focused on the critical question of sensitivity of SiGe BiCMOS technology to single event effects (SEEs) [1], when particles striking the transistors can cause the data to become temporarily or permanently corrupted. The temporary, or transient, SEEs are more problematic as the frequency of the circuit increases. Recent work [2], [3] has demonstrated that SiGe HBT logic from IBM and Jazz, as well as the IBM CMOS incorporated in the SiGe BiCMOS process all show significant sensitivity which varies with data rate and is often characterized by complex burst errors as opposed to single bit errors.

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P. Marshall is a NASA consultant, Brookneal, VA 24528 USA (e-mail: pwmarshall@aol.com).

M. Carts, M. Berg, and C. Siedleck are with Muniz Engineering, Inc., Houston, TX 77058 USA.

S. Currie, B. Randall, K. Fritz, and B. Gilbert are with the Mayo Foundation, Rochester, MN 55905 USA.

R. Reed is with Vanderbilt University, Nashville, TN 37235 USA.

K. Kennedy, R. Ladbury, C. Marshall, and K. LaBel are with the NASA Goddard Space Flight Center, Greenbelt, MD 20771 USA.

R. Krithivasan and J. Cressler are with the Georgia Institute of Technology, Atlanta, GA 30308 USA.

G. Niu is with Auburn University, Auburn, AL 36849 USA.

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II. Circuit for Radiation Effects Self Test (CREST)

Complex test equipment requirements and setup become increasingly expensive and difficult as data rates enter the multi-Gbits/s regime. This work describes a test chip architecture and implementation of a circuit to provide built-in self test to fully characterize both single bit and complex error modes in high speed logic. The Circuit for Radiation Effects Self Test (CREST) is demonstrated in IBM's 5AM HBT logic family. The 5AM self aligned HBT process is characterized by a 0.5 micron minimum feature size and f_T of 47 GHz. Our implementations of serial data registers include the baseline standard D flip-flop architecture as well as several other register designs under consideration for increased SEE hardness.

The CREST architecture allows for self testing at arbitrarily high data rates by taking advantage of the repeating nature of standard bit error rate test patterns. Pseudo-random numeric (PRN) patterns repeat every $2^n - 1$ bits, and a common value for n is 7 resulting in a pattern length of 127 bits. The shift register length incorporated in the CREST design is also 127 stages, and it is intended to operate with a repeating 127 bit data pattern as depicted in Fig. 1.

In error free operation and under the conditions of a 127 bit long register and a 127 bit long data sequence, the logic states of the input and output stages ought to remain constantly synchronized and identical. By comparing them for differences using a simple XOR gate, as depicted in Fig. 1, an indication of error (e.g., particle induced SEE) is obtained. This signal is latched as a flag to outside circuitry indicating that an error has been detected, and it is also used to stop all clock activity within the CREST circuit; preventing the bit stream which contains the error information from being flushed out of the shift register and lost. These functions are implemented according to the diagram shown as Fig. 2.

This implementation of the CREST contains, in addition to the previously mentioned shift register, other required elements. The clock-stop circuitry includes an anti-sliver functionality so

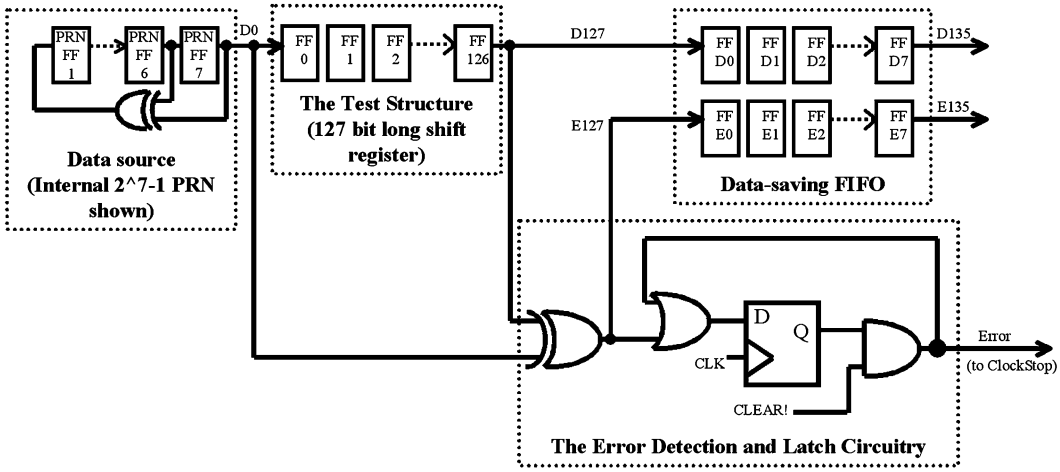


Fig. 1. The CREST autonomous error detection architecture.

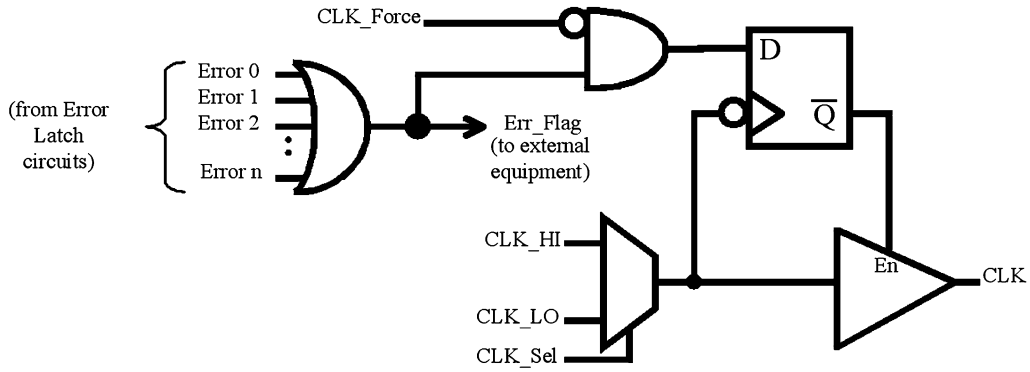


Fig. 2. Circuit implementation of the CREST Clock Stopping and Switching functions.

that at any clock speed only full clock pulses will propagate to the rest of the chip. Two clock inputs and a multiplexer to switch between them are provided so that a low speed clock can transmit the data stream out bit-by-bit for capture by sub-GHz equipment. External-input control signals to override the clock-stopping error flag, to clear the error flag, to select the clock source, etc. are also incorporated.

It takes a finite amount of time to detect an incorrect bit and stop the clock, so an additional short (7 stage) register follows the output of the 127 bit register. Also, as shown in Fig. 1, the output of the XOR gate used to detect error states feeds into another short register to indicate which bit(s) are in error. Thus, as seen in Fig. 1, two bit streams are available for capture bit by bit, by the external equipment: the D (data) bit stream and the E (error) bit stream. In addition, a 7-stage linear feed back register to generate the $2^7 - 1$ PRN (See Fig. 1) and a data-selecting multiplexer (not shown) are implemented on-chip to provide the option of feeding either internally or externally generated data.

The methodology of the CREST design can be implemented for a single shift register. However it was recognized that, with the addition of an OR gate as seen in Fig. 2, multiple shift registers could be implemented and simultaneously tested in parallel. CREST contains five shift registers built from different styles of master/slave D flip-flop configurations. The data input (D0) to each is from a common, either internal or external, PRN and the five different "Error" signals are combined logically via an "OR" gate as shown on the left side of Fig. 2 to generate the "Err_Flag" signal.

The five shift registers can be powered individually or in any combination. Each block of common circuitry (the PRN, the clock-stop circuitry, and others) are also discretely powered. All of CREST is implemented in current mode logic (CML) topology with current sources tied to the coupled emitters. Each block of circuitry has a common current mirror base terminal brought out of the chip.

In our test circuit, shift registers have been implemented with variations in the D flip-flop designs to determine which style may be most immune to SEEs. The five styles of flip flops are: 1) standard master-slave with 1 μm transistors and a nominal current of 0.6 mA, as shown in Fig. 3; 2) standard master-slave with 2.5 μm transistors and a higher current of 1.5 mA; 3) standard master-slave with triple-redundant 1 μm transistors (referred to as current shared hardened [2]) with a nominal current of 0.6 mA each (for a total of 1.8 mA); 4) dual-interleaved master-slave with 2.5 μm transistors and a higher current of 3 mA, as described in [4] and shown in Fig. 4; and 5) cross-coupled NAND gate with 1 μm transistors and a nominal current of 0.6 mA, as shown in Fig. 5. The CREST 5AM test chip also has four external ports available which can be used to interface with additional 127-bit shift registers that may have been implemented in a different technology without the self-checking features. This

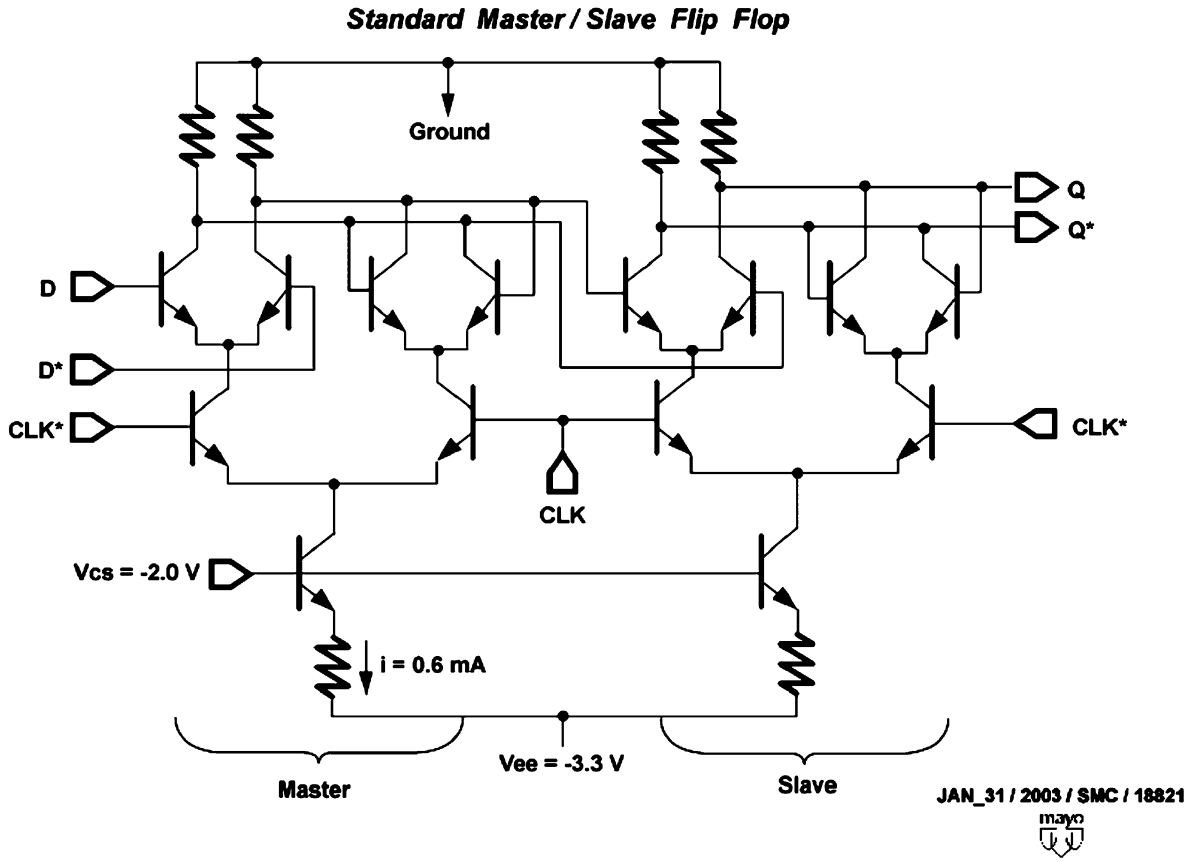


Fig. 3. Schematic of standard master slave flip flop.

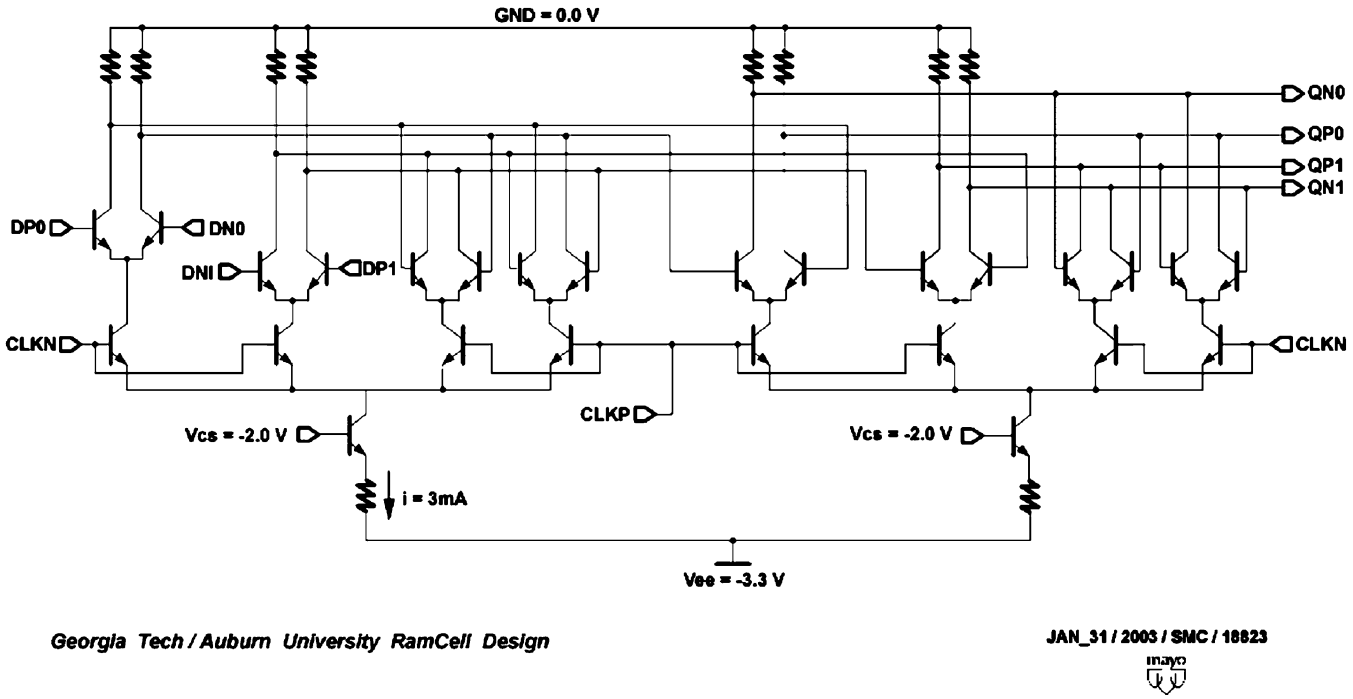


Fig. 4. Schematic of dual-interleaved master slave flip flop.

external interface is implemented through a multichip module, and both CML and Low Voltage Differential Signal (LVDS) levels are supported so that a "stand alone" 127 stage register can be tested.

The floor plan of the CREST design, including key interfaces, is presented in Fig. 6. The test vehicle was fabricated at IBM's commercial facilities in Burlington, VT, and our design was incorporated into a multiuser mask set through the services of MOSIS [5].

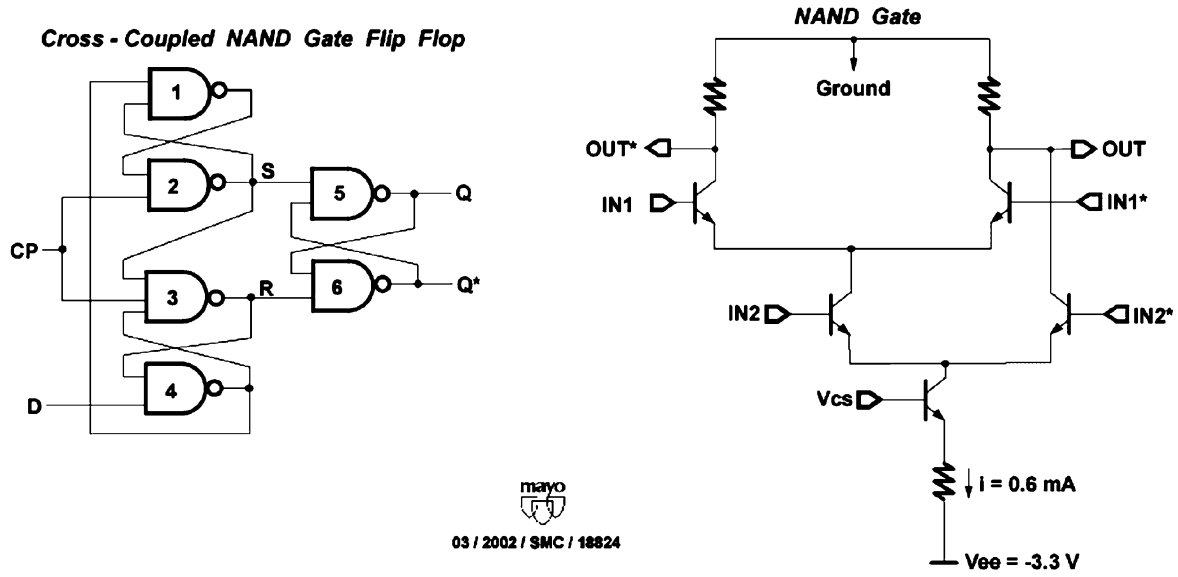


Fig. 5. Schematic of cross-coupled NAND gate flip flop and individual NAND gate.

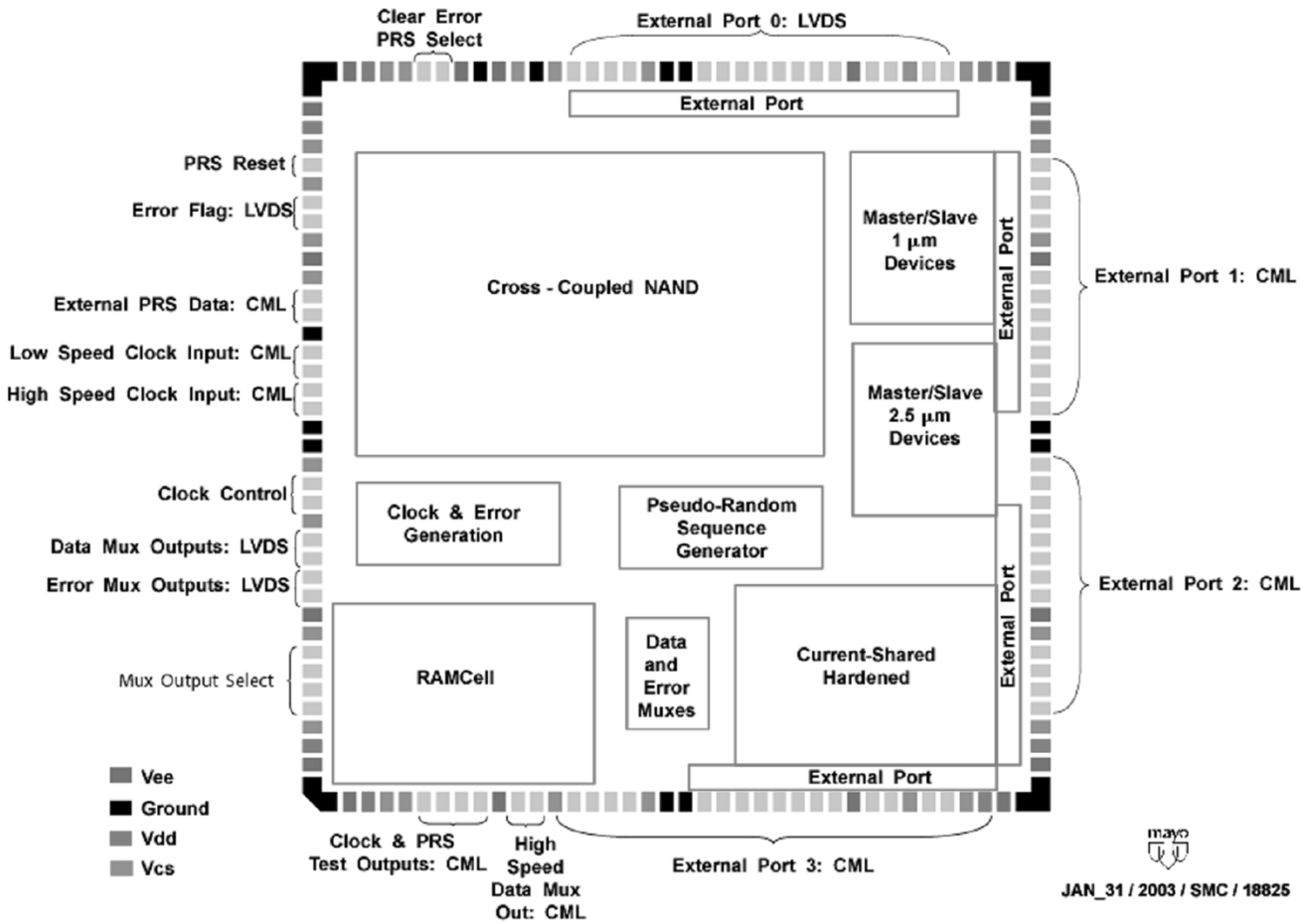


Fig. 6. Floor plan of circuit designed for evaluating SEEs containing five styles of flip flops and fabricated in the IBM 5AM technology.

III. FPGA Control of the CREST ASIC

The CREST ASIC's built-in error detection, clock halting and out-load circuitry operate at multi-Gbit/s rates, and normal PC data collection methods are extremely slow in comparison. To take better advantage of the CREST design's high speed performance, an FPGA-based printed circuit assembly was designed and built to initialize, arm and monitor the CREST for radiation sensitivity, and to very rapidly download data and initialize and rearm CREST when errors are detected.

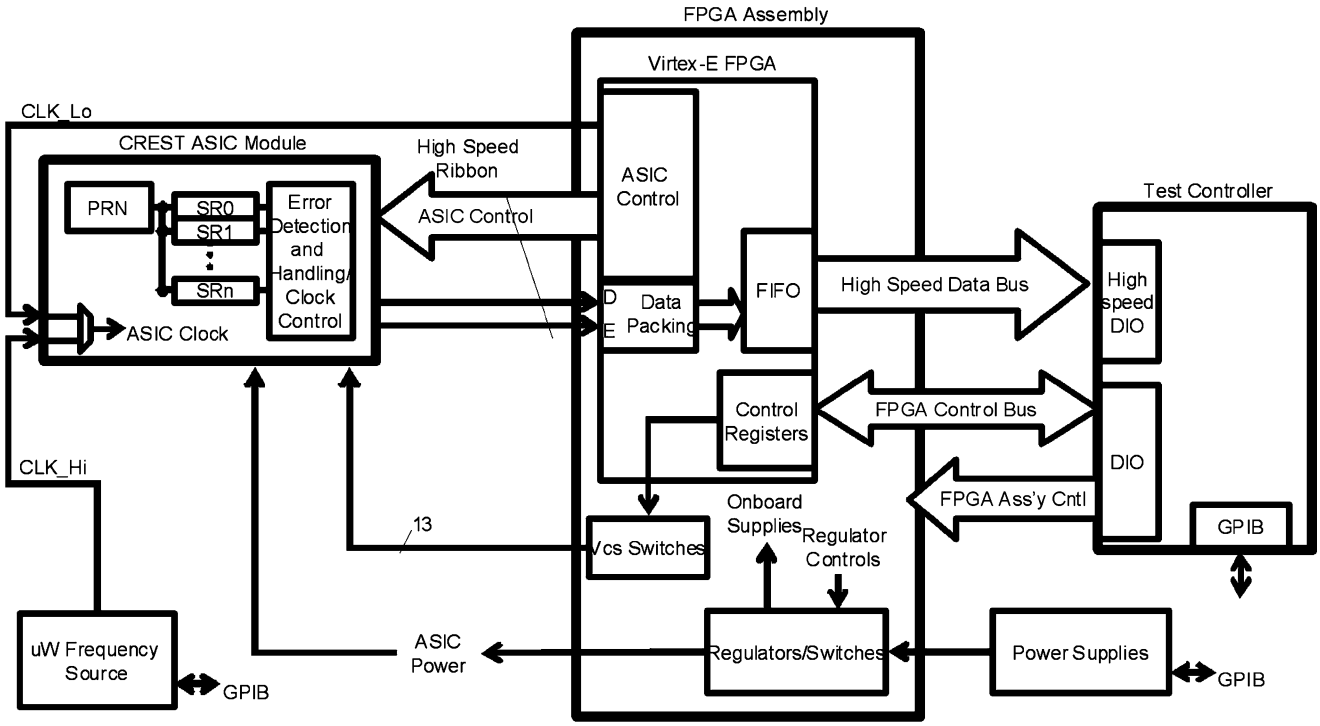


Fig. 7. The FPGA controlled version of the CREST minimizes the high speed interconnects, using only a single ended clock input into the CREST ASIC.

Additionally, as Fig. 7 demonstrates, the FPGA assembly interfaces with a PXI Controller and power sources and provides other functionality. The Test Controller is a PXI format PC with both traditional, 8255-like, digital input/output (DIO) and high-speed burst mode DIO (NI-6533). It communicates with the FPGA using two channels, a control register interface to set operating conditions and a dedicated high rate 16 bit parallel channel for data download. Upon power up the FPGA board is in a "Quiescent" mode, allowing parameters to be set. Once set into "ASICtest" mode, the FPGA automatically initializes it, and waits for error events to occur. It responds with a routine to download data from the CREST and pack it into 16 bit words before offloading them into a FIFO to decouple the test from the latency and slowness of the PXI Test Controller. Afterwards, the FPGA then initializes and rearms the CREST. The FPGA continues in this "ASICtest" mode until it is reset or power is removed.

The FPGA's FIFO controller maintains the "Start of Data Pointer" and "End of Data Pointer" so that the only handshaking from the Test Controller is an "ACK" bit, acknowledging that the current word has been read. The FPGA, in addition to its "Quiescent" mode and "ASICtest" mode, has a "RAMtest" mode to verify functionality of its memory, and a "Manual" control mode, so that individual outputs of the FPGA can be exercised manually.

Also implemented within the FPGA is a PRN pattern generator which can drive CREST's data input if desired. This feature was not needed in the testing reported here; however, it was included to allow the capability to provide data from a source outside the radiation environment. Along with this PRN an on-FPGA-assembly high-speed (by FPGA standards) clock and high-speed data and clock output translators allow for testing with a minimum of on-ASIC heat dissipation and external equipment if desired, for example while testing in vacuum.

The FPGA assembly also contains regulators which allow powering of various circuits, including the CREST Vee, Vdd and Vcs supplies, as well as some of the FPGA's own interfaces such as the Low Voltage Transistor-Transistor Logic (LVTTL) and Low Voltage CMOS (LVCMOS18) and Low Voltage Differential Signal (LVDS) I/O. Daughter cards provide for the powering and resetting of an external (truly) high speed PRN generator, the translation of CML output signals, and the safe switching of the CREST ASIC's Vcs (Voltages to current sources) signals.

One advantage of using the FPGA controlled test approach is that data can be gathered much quicker than standard BERT equipment can gather and download bit-by-bit information. This FPGA assembly has the potential for running at an internal clock rate of hundreds of MHz but for the purposes of proving the system it was developed to run at a clock rate of 1 MHz to avoid any possible propagation delay and skew problems. Nonetheless, the time to download and reinitialize the CREST ASIC was approximately 250 us, suggesting that the maximum event rate ought to be kept below 1000 events per second. In our testing, we logged full error histories at rates in the tens to hundreds per second, and viewed event counts and error statistics in real time with a $\sim$10 Hz update of the monitor PC. This capability is important for the task of acquiring large error sample sets to properly characterize the complex error modes seen in high speed shift register testing [2]. And, this offers a significant advantage over the maximum BERT-based data gathering rate of approximately one or two events per second, as much longer intervals are needed for clearing and rearming typical BERT equipment.

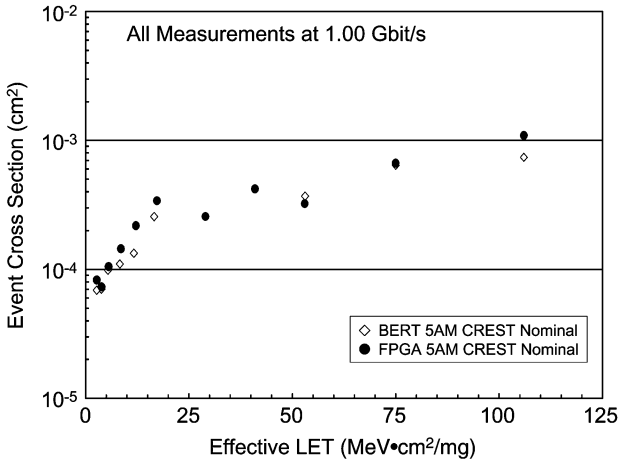


Fig. 8. The baseline 1 μm transistor with 0.6 mA switching current register of Fig. 3 shows essential identical response to heavy ions when tested with the FPGA controller versus the commercial BERT equipment.

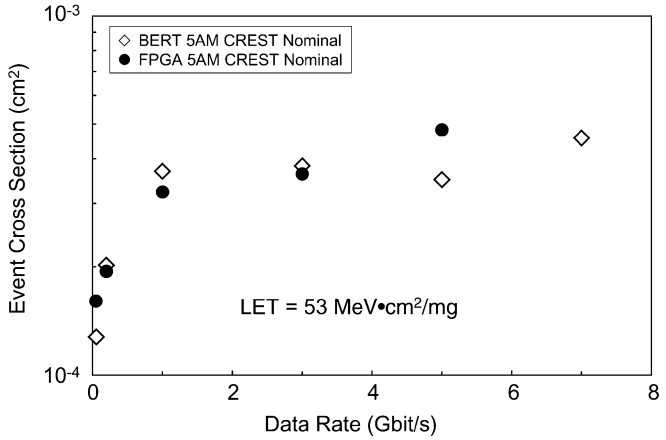


Fig. 9. The baseline 1 μm transistor with 0.6 mA switching current register of Fig. 3 shows essential identical response to heavy ions when tested with the FPGA controller versus the commercial BERT equipment. Trends with data rate are steep below 1 Gbit/s.

IV. Results and Discussion

The 5AM SiGe CREST ASIC has now been thoroughly explored through both broad beam heavy ion tests at Texas A&M University's cyclotron and micro-probing using laser testing with the Naval Research Lab (NRL) pulsed laser. Our data set is comprised of 288 heavy ion test runs exercising the CREST ASIC with conventional BERT equipment, 190 test runs probing individual circuit elements of the various D flip-flop designs using the laser, and an additional 328 runs using heavy ions while operating the CREST under FPGA control. The data set exceeds 10^5 errors representing a range of error complexity, ion species and trajectories, data rates from 50 Mbits/s to the maximum operating rate of a given circuit, and most importantly a variety of configurations of the CREST ASIC. This section will present representative data to both demonstrate validation of the CREST approach, and investigate important findings showing the response of the five 5AM SiGe circuit design architectures.

Heavy ion test results of the nominal 1 μm register design are presented in Figs. 8 and 9. Fig. 8 compares the event cross sections at 1 Gbit/s versus effective LET, and as in [2] an event is defined as a single bit error or string of related bit errors. In this plot, conventional geometric considerations describing the sensitive volume as a Rectangular Parallelepiped (RPP) have been assumed where off-normal incidence angles are involved. The two data sets plotted compare two identical test articles, but with one CREST test under FPGA control and the other using an external PRN data sequence generator and an Anritsu model MP1764A pattern detector (a.k.a. BERT). Agreement between the two data sets confirms that the autonomous FPGA-based operation of the CREST can indeed produce reliable measurements. The response is characterized by a very low threshold and very large device event cross section at higher LETs, indicating significant sensitivity to heavy ion SEEs and suggesting the likelihood of proton sensitivity as well.

Note that for this 127 stage register, the large device cross section approaching 10^{-3} cm^2 at high LETs implies a sensitive area of almost 800 μm^2 per register stage. Given the simplicity and low transistor count of the design (Fig. 3), and the fact that our circuit analyzes indicate only a fraction of the transistors will dominate the sensitivity, the effective sensitive area per sensitive node appears to be hundreds of μm^2 for the 1 Gbit/s case. The deep trench isolation for the 5AM process results in confinement of the collector-substrate junction of an area of only $\sim 20\,\mu$m^2, and this suggests that charge diffusion in the substrate plays a major role in the SEE response of the 5AM process. Similar arguments [2], and microbeam studies [6] on the IBM 7HP process have led to similar conclusions.

Upon close inspection, the data of Fig. 8 show differences between the two data sets attributable mostly to scatter, but with the FPGA controlled results showing a slightly higher cross section at eight of the nine effective LETs where comparisons are possible. We note that in the BERT-based version of the test, only the 127 stage data register is effectively under test, whereas in the FPGA version the additional circuit elements (PRN generator, XOR logic, output FIFO, etc, are involved). We estimate an expected $\sim 25\%$ increase in the sensitivity due to this additional circuitry, and hence the slight increase in cross section. As will be discussed later, the CREST method has been implemented with the ability to identify errors generated within these individual circuit blocks, and this is important as they are in no way hardened against contributing to the overall error count. We also note that because the FPGA test involved these additional circuit functions, the CREST ASIC required more power and ran warmer in those tests. This limited the maximum data rate to 5 Gbit/s in that case, and no comparison was possible at the 7 Gbit/s rate. Similar thermal issues prevented the testing of the cross-coupled nand implementation (Fig. 5) with the FPGA control and limited the data rate with BERT equipment to 4.5 Gbit/s, but on the other four register designs examined the FPGA and BERT-based tests produced essentially identical results.

Fig. 9 compares FPGA and BERT-based CREST ASIC test results showing how the 5AM event cross section tends with data rate, again for the case of the baseline design (Fig. 3) and at a constant LET of 53 MeV-cm^2/mg. Note the close agreement for the two test techniques, and the steep rise in cross section below 1 Gbit/s. The apparent saturation in the event cross section above 1 Gbit/s suggests a characteristic time constant for charge collection of $\sim$1 ns, as in the case of 7HP SiGe [2].

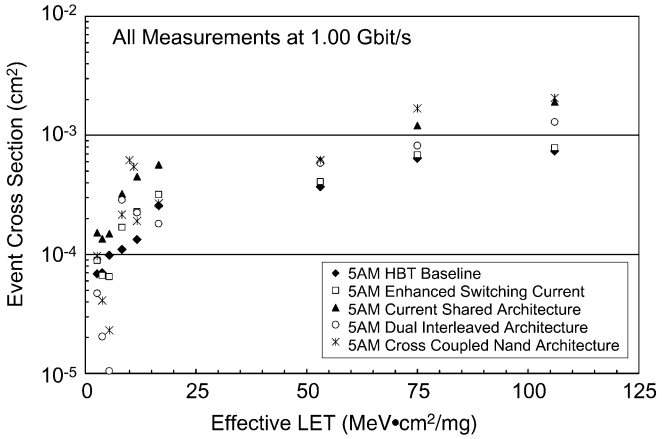


Fig. 10. The event cross section varies similarly with LET for the 5 register designs, with the exception of the angular effects near the threshold.

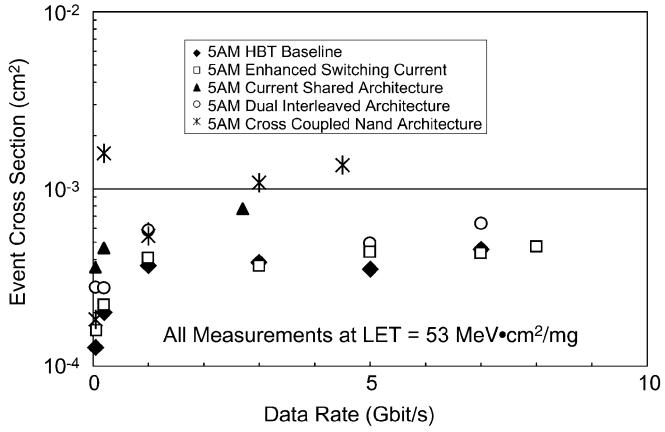


Fig. 11. Event cross section versus data rate.

Results comparing the cross section dependence on effective LET for the five register designs are shown as Fig. 10. These data, acquired at 1 Gbit/s, show trends characterized by low threshold LET and large cross sections at high LET. Given the significant differences in circuit design, power dissipation, transistor size and count, and real estate (Fig. 6); the most remarkable result is that the register-to-register differences are so minor. In each register, the event cross section continues to increase even at large effective LET, again implicating the importance of charge diffusion in the substrate. The one notable difference among registers involves the measurements taken at angle. Though not distinguished in the figure, four ion species were used, and measurements were taken at 45 and 60 degrees in addition to normal incidence. At normal incidence, the Ne, Ar, Kr, and Xe LETs were 2.7, 8.6, 29, and 53 MeV-cm^2/mg respectively. Especially near the threshold, the RPP assumptions applied to generate the figure clearly break down for some register designs; even though all registers were fabricated in the same process: even on the same die! More detailed interpretation and consequences of this will be explored later in this section.

Trends comparing the five registers event cross sections versus data rate at a constant LET of 53 MeV-cm^2/mg are shown as Fig. 11. For all registers, the steepest rise occurs below 1 Gbit/s, and the cross-coupled NAND and current shared cell types continue to increase at higher data rates. Here, the sensitivity appears to correlate with the transistor count and circuit complexity (see the relative real estate allocations in Fig. 6).

A. Capture and Analyzes of Complex Error Signatures

As previously noted [2], event cross sections offer only partial insight into the understanding of the sometimes complex error bursts seen in high speed digital logic. As errors were flagged and read first into the FPGA and then onto the PXI controller's hard drive, they were time tagged and stored as two parallel bit streams consisting of 135 pairs of "Data" bits and corresponding "Error" bits. Nominally, if the "E(rror)" bit is set the value of its corresponding "D(ata)" bit is considered to be in error. However, since the entirety of the data generation, shifting, and comparison circuitry is within the particle beam a variety of error sources are in play. Considerations such as this were kept in mind as the data was analyzed. By capturing the complete contents of the data registers and PRN, it is possible to fully reconstruct the "correct" state of the data sequence, and precisely determine the morphology of almost all error bursts.

The error analysis software is written in c++, and it can be used to operate on errors either in real time, or in post-processing. In either case, each error is screened against a set of known error types. In some cases there is ambiguity as to the physical location of the error origination (e.g., single bit flips and short bursts may arise from either data register hits or clock distribution node hits), but more often the type of error very strongly suggest specific origins.

Fig. 1 shows a simplified data path for one shift register from the PRN to the "D" and "E" bit outputs. By design the largest cross section within the CREST will be in the 127 bit shift register under test, but other circuits are also susceptible to some degree. For example, errors were gathered only when the error flag was raised but some errors had no erroneous bits. This indicates hits affecting the comparison XOR gate's output node. Such hits would set the Err_Flag bit and stop the clock, resulting in the gathering of 135 bits of correct data. These were seen; they were filtered out first and categorized as "Misfire" errors.

Errors were gathered that had one erroneous bit followed by a second erroneous bit exactly one pattern later, of the opposite polarity. It is impossible that one bit can flip both directions but it can be seen that if the output of the PRN has a single bit error the XOR gate will indicate a difference from the bit that preceded it by 127 bits. Then, 127 bits later the erroneous bit will cause another difference indication. The unique characteristic of this type of error made its identification very easy. These "D0" errors, named after the node in which they occur, were filtered next.

Single bit errors, which indeed accounted for a vast majority of error events, could occur in almost any part of the data path, and even some parts of the clock signal path. While it is highly unlikely they would occur within the trailing FIFOs of 7 flip-flops (because they would be flushed and lost without Err_Flag being raised) they do occur in a location that produces distinct signatures, the difference comparing XOR gate. If the XOR gate itself is hit and causes an "E" bit to be set and an error to be generated where the data stream was not actually in error, it can be detected because the PRN data stream is predictable. Fig. 1 shows that the value of each bit generated in the PRN can be calculated by the value of the

sixth and seventh bits preceding it. Similarly it can be calculated by the next bit following it and the seventh bit following it; this definition is equivalent but more useful since the first bit of interest in a gathered error event is usually less than seven bits from the beginning of the bit stream. Single bit errors are checked against the error definition for "XOR" errors. If they do not match they are categorized as "Singles".

One multiple bit error type commonly expected is a flattening of the data stream either to logic zero or logic one for some period of time. While these might properly be considered to be entirely distinct in type from the standard single bit flip (in which case the "Singles" category would be expected to incorrectly include some flattening type of errors lasting only one bit long) we categorized as "Zeros" and "Ones" only multiple bit errors where the erroneous bits were all either ones or zeros and did not try to calculate what fraction of "Singles" might be "Ones" and "Zeros".

The PRN is a state machine stepping from one of its 128 possible states stored in its seven flip-flops to another in orderly sequence. If one of these flip-flops is hit, it will cause the PRN state (and thus the bit stream) to not step to the next state but instead to jump to some other state. It will not return to its original synchronization but will continue forever from its new state. This manifests itself in the collected data as a high error rate continuing through the end of the collected record. Immediately following this error condition, the output of the shift register follows the old synchronization while the input follows the new. If a longer bit stream were collected the errors would cease as the newly synchronized bit stream reached the shift register output. Errors of this type were checked to identify whether the high error portion of the data fit a different synchronization with low or zero errors. Again, this "S(ingle) Shift" type is indicative of a hit to the seven flip-flops of the PRN.

After errors of all these types had been filtered, a minor portion of all error events remained. While some have fairly distinct signatures they are not currently understood to be generated by a particular circuit mechanism or at a certain location and are thus categorized as a single type, "Other".

This categorization results in 13 distinct error categories, and their relative occurrences do change according to the data rate and effective LET. The most notable trend is that single bit errors which dominate at low LET and low data rate become less frequent as multiple bit errors dominate at high LET and high data rate. This trend is reflected in Table I for the four register types tested with the FPGA controlled CREST. The Table also indicates that only minor changes in burst error morphology are noted when comparing the four register designs.

TABLE I
COMPARISON OF ERROR LENGTHS FOR 4 REGISTER TYPES

DUT	Data Rate (Gbit/s)	LET (MeVcm^2/mg)	Event Cross section (cm^2)	average error length (ns)	average bit errors per event (bits)
1	0.2	2.7	8.25E-05	21.5	2.1
2	0.2	2.7	1.03E-04	45.5	4.8
3	0.2	2.7	1.76E-04	36.5	3.2
4	0.2	2.7	7.60E-05	33	3.4
1	0.2	53	3.23E-04	50	5.0
2	0.2	53	4.12E-04	51	5.0
3	0.2	53	7.09E-04	41	4.1
4	0.2	53	5.54E-04	46	3.7
1	3	2.7	1.22E-04	3.9	6.4
2	3	2.7	1.42E-04	3.1	4.7
3	2.5	2.7	2.36E-04	7	7.8
4	3	2.7	9.95E-05	4.4	7.1
1	3	53	4.08E-04	8.6	11.2
2	3	53	4.80E-04	6.9	9.6
3	2.5	53	1.11E-03	9	11.4
4	3	53	6.08E-04	6.9	10.3

B. Discussion of Angular Dependence

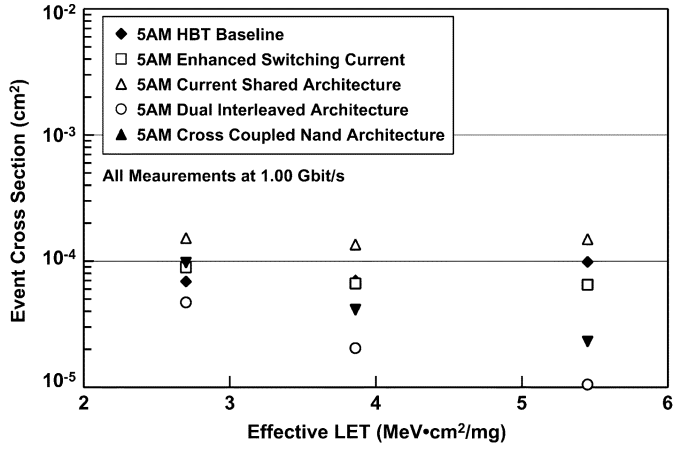
Extraordinary differences appear in the trend with effective LET as the angle of incidence changes from normal to 45 and 60 degrees for Ne-22. This is further explored in Fig. 12. Part (a) of the figure shows the data for Ne at 0, 45 and 60 degrees plotted with RPP assumptions with respect to adjusted fluence and effective LET, as in Fig. 10. Clearly, the RPP assumptions do not work here. In Fig. 12(b), these data are replotted to show the normalized event cross section at various incident angles. The data are normalized to the event cross section at normal incidence for each circuit and the RPP correction to fluence was not applied to these data. (The cross section is simply the ratio of number of observed errors to the normally incident particle fluence.) The dashed line gives the cosine of the angle of incidence. If the first-order RPP assumption is applicable then the normalized data would fall on or above the cosine function, and this follows from the fluence adjustment made when plotting data according to RPP assumptions. Effective LET considerations would drive the data points further above the cosine trend line.

The baseline (register 1) cross sections falls slightly above the cosine function, all others fall below this function. The enhanced switching current (register 2) and current-shared architecture circuits (register 3) both fall slightly below the cosine function The dual-interleaved (register 4) and cross-coupled NAND cells (register 5) result in the most dramatic departure from the first-order RPP assumption. This anomalous behavior is consistent with previously noted trends in other SiGe technologies described in [1], [2], [6].

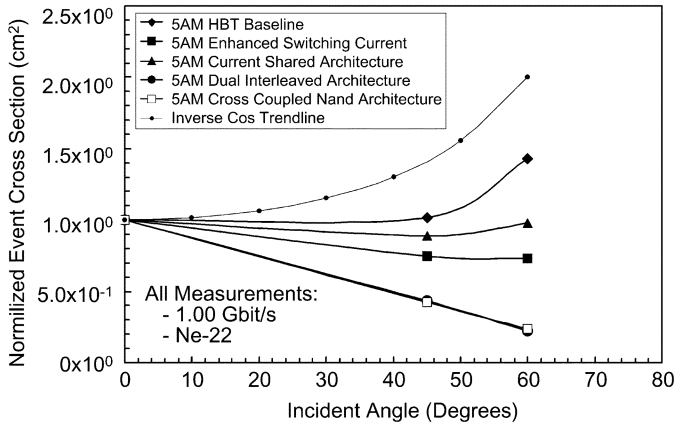
Quasimixed-mode 3-D simulations [4], [7] predict that register types 2 and 3 would have a similar critical charge for SEU, and types 4 and 5 would have similar, yet larger critical charge for upset. The baseline master-slave flip-flop design was predicted to have the lowest critical charge.

Recent simulations similar to those in [8] on IBM SiGe 5HP HBT show that normally incident ions typically yield more charge collection than ions at any other angle. This reduction in charge collection over angle is believed to be, in part, the cause for the apparent anomalous angular response.

Qualitative understanding about the interplay between the charge collected over angle and the circuit critical charge can be gained from the data in Fig. 12. Given the assumptions about the critical charges of each circuit in Fig. 12, and the fact that



(a)



(b)

Fig. 12. Part (a) replots the data of Fig. 10 on an expanded abscissa to show Ne at 0, 45, and 60 degree incidence with RPP assumptions. (b) Shows these data normalized and without RPP assumptions, along with the cosine trend line for comparison.

less charge is collected at any angle other than zero degrees, it is easy to understand the trends seen in the data at low LET. For example, it is expected that register type 5 has a lower cross-section at low charge depositions (low effective LET) than the baseline. Less charge is collected at 60 degrees than at zero degrees. So, one could expect a larger reduction in cross-section for register type 5 relative to the baseline.

In fact, the baseline cross section increases in comparison with the cosine function. This could possibly be due to the increased sensitivity of these circuits to events occurring outside the trench area [2], [6].

A detailed understanding of the angle response is required for accurate on-orbit performance predictions. In space, particles arrive at all angles of incidence; if the response over angle can be mitigated to less than the cosine function, then the on-orbit rate will be reduced. It is easy to see from Fig. 12 that the on-orbit SEU rate will be significantly lower for registers 4 and 5 than for the other registers. A quantified discussion on these angular effects is an area of active research, but we note that for omnidirectional flux, half the particles will arrive with trajectories within 30 degrees of the device plane. As our 60 degree data for register types 4 and 5 are already reduced by nearly 10x at 60 degree incidence, we recognize that their on-orbit error rates would likely be decreased by at least 10x relative to the baseline register type 1.

V. Summary

We describe the implementation of a high speed SEE self test architecture and present the first reported data on IBM's 5AM logic family, along with the SEE characteristics of five different variations of the D flip-flop architecture. By migrating the majority of the high speed interconnection from the bench test equipment and into the ASIC design, we solve the difficult problem of controlling critical timing paths for broadband testing and greatly reduce test development costs. In addition, we attain a more efficient means of acquiring large data sets to fully characterize a given technology or circuit type, thereby reducing accelerator test time.

To date, we have implemented variants of the basic CREST shift register design in the following technologies: IBM 5AM (47 GHz f_T HBT with 0.5 μm CMOS), IBM 7HP (120 GHz f_T HBT with 0.18 μm CMOS), and Jazz SiGe120 (150 GHz f_T HBT with 0.18 μm CMOS), and IBM 8HP (200 GHz f_T HBT with 0.13 μm CMOS). These successful test results in 5AM demonstrate the general applicability and advantages of the CREST approach.

Within the 5 register designs we investigated, we noted a surprisingly similarity in the overall SEE event cross section, but striking differences with respect to angular effects. Taking this into account, we recognize that SEEs in this SiGe technology reflect the interplay of the technology as well as circuit dependent variables. By reducing the sensitivity to off-normal ion strikes, order-of-magnitude reductions in upset rates can be achieved.

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